IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Serial No:	09/655,755	§	Examiner:	Edith M. Chang
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For: Digital Filter Design

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APPEAL UNDER 35 U.S.C. §134

This Brief is submitted in connection with the decision of the Primary Examiner set forth in the Final Official Action dated December 5, 2005, finally rejecting claims 1-22.

Real Party in Interest

The real party in interest, by assignment, is: Telefonaktiebolaget LM Ericsson (publ)
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Stockholm, Sweden

Related Appeals and Interferences

None.

Status of Claims

Claims 1-22 are pending in the present application, each of which are finally rejected and form the basis for this Appeal. Claims 1-4, 7-8, 10, 13-14, 17-18 and 20,

stand rejected, under 35 U.S.C. §103(a), as being unpatentable over Freed (US 5,686,683) in view of Levien (US 5,337,264); claims 5 and 15 stand rejected, under 35 U.S.C. §103(a), as being unpatentable over Freed in view of Levien and further in view of Leitch (US 5,202,900); claims 6, 9, 16 and 19 stand rejected, under 35 U.S.C. §103(a); as being unpatentable over Freed in view of Levien and further in view of Craven (US 5,548,286); and, claims 11, 12, 21 and 22 stand rejected, under 35 U.S.C. §103(a), as being unpatentable over Freed in view of Levien and further in view of Picchi, *et al.* (US 4,547,889).

Status of Amendments

The claims set out in the Claims Appendix include all entered amendments. No amendment has been filed subsequent to the final rejection.

Summary of Claimed Subject Matter

Claim 1

Claim Element	Specification Reference
1. (Previously Presented) A method of designing a digital filter, including the steps of:	Figure 24 and description relating thereto.
first, determining a real-valued discrete-frequency representation of a desired full length digital filter;	Figure 24 and description relating thereto; Page 7, line 29, to page 9, line 2
second, transforming said real-valued discrete-frequency representation into a corresponding discrete-time representation;	Figure 24 and description relating thereto; Page 9, lines 2-9.
third, circularly shifting said discrete-time representation; and	Figure 24 and description relating thereto; Page 9, line 25, to page 10, line 3.
fourth, applying a shortening window to said discrete-time representation to produce a zero-padded reduced length filter.	Figure 24 and description relating thereto; Page 10, lines 5-16.

Claim 7

Claim Element	Specification Reference
7. (Previously Presented) A digital convolution method, including the steps of:	Figure 24 and description relating thereto.

first, determining a real-valued discrete-frequency representation of a desired full length digital filter;	Figure 24 and description relating thereto; Page 7, line 29, to page 9, line 2
second, transforming said real-valued discrete-frequency representation into a corresponding discrete-time representation;	Figure 24 and description relating thereto; Page 9, lines 2-9.
third, circularly shifting said discrete-time representation;	Figure 24 and description relating thereto; Page 9, line 25, to page 10, line 3.
fourth, applying a shortening window to said discrete-time representation to produce a zero-padded reduced length filter; and	Figure 24 and description relating thereto; Page 10, lines 5-16.
fifth, convolving an input signal with said zero-padded reduced length filter.	Figure 24 and description relating thereto; Page 13, lines 25-26.

Claim 13

Claim Element	Specification Reference
13. (Previously Presented) A digital filter design apparatus, including:	Figures 24 and 25 and description relating thereto.
means for determining a real-valued discrete-frequency representation of a desired full length digital filter;	Figures 24 and 25 and description relating thereto; Page 7, line 29, to page 9, line 2
means, coupled to the output of said means for determining a real-valued discrete-frequency representation, for transforming said real-valued discrete-frequency representation into a corresponding discrete-time representation;	Figures 24 and 25 and description relating thereto; Page 9, lines 2-9.
means, coupled to the output of said means for transforming said real-valued discrete-frequency representation, for circularly shifting said discrete-time representation; and	Figures 24 and 25 and description relating thereto; Page 9, line 25, to page 10, line 3.
means, coupled to the output of said means for circularly shifting said discrete-time representation, for applying a shortening window to said discrete-time representation to produce a zero-padded reduced length filter.	Figures 24 and 25 and description relating thereto; Page 10, lines 5-16.

Claim 17

Claim Element	Specification Reference
17. (Previously Presented) A digital convolution apparatus, including: means for determining a real-valued discrete-frequency representation of a desired	Figures 24 and 25 and description relating thereto.

full length digital filter;	
means, coupled to the output of said means for determining a real-valued discrete-frequency representation, for transforming said real-valued discrete-frequency representation into a corresponding discrete-time representation;	Figures 24 and 25 and description relating thereto; Page 7, line 29, to page 9, line 2; Page 9, lines 2-9.
means, coupled to the output of said means for transforming said real-valued discrete-frequency representation, for circularly shifting said discrete-time representation;	Figures 24 and 25 and description relating thereto; Page 9, line 25, to page 10, line 3.
means, coupled to the output of said means for circularly shifting said discrete-time representation, for applying a shortening window to said discrete-time representation to produce a zero-padded reduced length filter; and	Figures 24 and 25 and description relating thereto; Page 10, lines 5-16.
means, coupled to the output of said means for applying a shortening window to said discrete-time representation, for convolving an input signal with said zero-padded reduced length filter.	Figures 24 and 25 and description relating thereto; Page 13, lines 25-26.

The specification references listed above are provided solely to comply with the USPTO's current regulations regarding appeal briefs. The use of such references should not be interpreted to limit the scope of the claims to such references, nor to limit the scope of the claimed invention in any manner.

Grounds of Rejection to be Reviewed on Appeal

1.) Claims 1-4, 7-8, 10, 13-14, 17-18 and 20, stand rejected, under 35 U.S.C. §103(a), as being unpatentable over Freed (US 5,686,683) in view of Levien (US 5,337,264).

2.) Claims 5 and 15 stand rejected, under 35 U.S.C. § 103(a), as being unpatentable Freed in view of Levien and further in view of Leitch (US 5,202,900).

3.) Claims 6, 9, 16 and 19 stand rejected, under 35 U.S.C. §103(a), as being unpatentable over Freed in view of Levien and further in view of Craven (US 5,548,286).

4.) Claims 11, 12, 21 and 22 stand rejected, under 35 U.S.C. §103(a), as being unpatentable over Freed in view of Levien and further in view of Picchi, *et al.* (US 4,547,889).

Argument

1.) Rejection of claims 1-4, 7-8, 10, 13-14, 17-18 and 20 as being unpatentable over Freed (US 5,686,683) in view of Levien (US 5,337,264)

The Examiner rejected claims 1-4, 7-8, 10, 13-14, 17-18 and 20 as being unpatentable over Freed (US 5,686,683) in view of Levien (US 5,337,264). The Applicant traverses the rejections.

Freed addresses a fundamentally different problem than the claimed invention and, thus, is not an appropriate prior art reference. Applicant's invention is directed to designing a digital filter, *e.g.*, H(z), from a given spectrum characteristic. The filter is applied to a signal in order to produce a desired filtering operation. Mathematically, the Applicant's invention treats the problem of designing a filter, H(z), that produces a desired output, y(t), when applied to a signal, x(t): in other words, y(t) = H(z)x(t). In contrast, Freed is directed to the generation of an artificial signal from a given spectrum characteristic, which mathematically can be expressed as generating a signal y(t) without any input signal; *i.e.*, y(t) = IFFT(H(f)).

The Examiner states that Freed, together with Levien, teaches the steps in claim 1. Claim 1, however, is directed to the design of a digital filter, whereas Freed is directed to designing a signal (*i.e.*, "sound synthesis"). Despite the fundamentally different problem areas addressed by Applicant's invention and Freed, however, some steps are similar. For example, the first two steps of claim 1 ("determining a real-valued discrete-frequency representation of a desired full length filter" and "transforming said real-valued discrete frequency representation into a corresponding discrete-time representation") are similar or identical to processes described by Freed. The third and fourth steps of claim 1, however, are not described by Freed or Levien.

In contrast to the Examiner's assertion, the third and fourth steps of claim 1 are not linked to any overlap-add technique. An overlap-add technique is used by frequency

domain implementation of filtering operations (or signal generations), as described on page 5, line 18, to page 7, line 27. Claim 1, however, treats the problem of designing the filter used in this filtering operation, not the filtering operation itself. Steps three and four in claim 1 define a procedure of obtaining a filter with the desired properties with respect to length of the filter and phase response, as described on page 9, line 28, to page 10, line 25; the benefits of the filter characteristics is explained on page 10, line 27, to page 11, line 7. Steps three and four of claim 1, however, cannot be implemented via an overlap-add technique and, thus, are not disclosed by the overlap-add techniques of Freed and Levien. Furthermore, there is not teaching or suggestion in Freed or Levien to combine their respective teachings to arrive at the novel combination of operations recited in claim 1. Accordingly, the Examiner has failed to establish a *prima facie* case of obvious of claim 1.

Whereas independent claims 7, 13, and 17 recite limitations analogous to those of claim 1, those claims are also not obvious over Freed in view of Levien. Furthermore, whereas claims 2-6 are dependent from claim 1, claims 8-12 are dependent from claim 7, claims 14-16 are dependent from claim 13, and claims 18-22 are dependent from claim 17, and include the limitations of their respective base claims, those claims are also not obvious over Freed in view of Levien.

2.) Rejection of claims 5 and 15 as being unpatentable over Freed in view of Levien and further in view of Leitch (US 5,202,900)

Claims 5 and 15 are dependent from claims 1 and 13, respectively, and include the limitations of their respective base claims. Therefore, whereas claims 1 and 13 have been shown *supra* to be patentable, claims 5 and 15 are likewise patentable.

3.) Rejection of claims 6, 9, 16 and 19 as being unpatentable over Freed in view of Levien and further in view of Craven (US 5,548,286)

Claims 6, 9, 16 and 19 are dependent from claims 1, 7, 13 and 19, respectively, and include the limitations of their respective base claims. Therefore, whereas claims 1, 7, 13 and 19 have been shown *supra* to be patentable, claims 6, 9, 16 and 19 are likewise patentable.

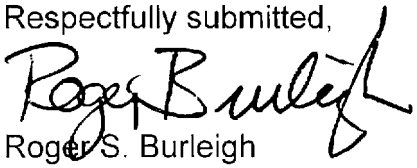
4.) Rejection of claims 11, 12, 21 and 22 as being unpatentable over Freed in view of Levien and further in view of Picchi, *et al.* (US 4,547,889)

Claims 11-12 and 21-22 are dependent from claims 7 and 17, respectively, and include the limitations of their respective base claims. Therefore, whereas claims 7 and 17 have been shown *supra* to be patentable, claims 11-12 and 21-22 are likewise patentable.

CONCLUSION

In view of the foregoing remarks, the Applicants believe all of the claims currently pending in the Application to be in a condition for allowance. The Applicants, therefore, respectfully request that the Board revere the Examiner's claim rejections.

Respectfully submitted,



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CLAIMS APPENDIX

1. (Previously Presented) A method of designing a digital filter, including the steps of:

first, determining a real-valued discrete-frequency representation of a desired full length digital filter;

second, transforming said real-valued discrete-frequency representation into a corresponding discrete-time representation;

third, circularly shifting said discrete-time representation; and

fourth, applying a shortening window to said discrete-time representation to produce a zero-padded reduced length filter.

2. (Previously Presented) The method of claim 1, further including the step of circularly shifting said zero-padded reduced length filter to remove leading zeroes.

3. (Previously Presented) The method of claim 1, wherein said real-valued discrete-frequency representation is formed by a noise suppressing spectral subtraction algorithm.

4. (Previously Presented) The method of claim 1, wherein said real-valued discrete-frequency representation is formed by a frequency selective non-linear algorithm for echo cancellation.

5. (Previously Presented) The method of claim 1, wherein said shortening window is a Kaiser window.

6. (Previously Presented) The method of claim 1, further including the step of transforming said zero-padded reduced length filter into a minimum phase filter.

7. (Previously Presented) A digital convolution method, including the steps of:

first, determining a real-valued discrete-frequency representation of a desired full length digital filter;

second, transforming said real-valued discrete-frequency representation into a corresponding discrete-time representation;

third, circularly shifting said discrete-time representation;

fourth, applying a shortening window to said discrete-time representation to produce a zero-padded reduced length filter; and

fifth, convolving an input signal with said zero-padded reduced length filter.

8. (Previously Presented) The method of claim 7, further including the step of circularly shifting said zero-padded reduced length filter to remove leading zeroes.

9. (Previously Presented) The method of claims 7, further including the step of transforming said zero-padded reduced length filter into a minimum phase filter.

10. (Previously Presented) The method of claim 7, wherein the step of convolving includes the step of performing a convolution in the time domain using the discrete-time representation of said zero-padded reduced length filter.

11. (Previously Presented) The method of claim 7, wherein the step of convolving includes the step of performing a convolution in the frequency domain by using an overlap-add method.

12. (Previously Presented) The method of claim 7, wherein the step of convolving includes the step of performing a convolution in the frequency domain by using an overlap-save method.

13. (Previously Presented) A digital filter design apparatus, including:

means for determining a real-valued discrete-frequency representation of a desired full length digital filter;

means, coupled to the output of said means for determining a real-valued discrete-frequency representation, for transforming said real-valued discrete-frequency representation into a corresponding discrete-time representation;

means, coupled to the output of said means for transforming said real-valued discrete-frequency representation, for circularly shifting said discrete-time representation; and

means, coupled to the output of said means for circularly shifting said discrete-time representation, for applying a shortening window to said discrete-time representation to produce a zero-padded reduced length filter.

14. (Previously Presented) The apparatus of claim 13, further including means for circularly shifting said zero-padded reduced length filter to remove leading zeroes.

15. (Previously Presented) The apparatus of claim 13, wherein the shortening window applying means implements a Kaiser window.

16. (Previously Presented) The apparatus of claim 13, further including means for transforming said zero-padded reduced length filter into a minimum phase filter.

17. (Previously Presented) A digital convolution apparatus, including:

means for determining a real-valued discrete-frequency representation of a desired full length digital filter;

means, coupled to the output of said means for determining a real-valued discrete-frequency representation, for transforming said real-valued discrete-frequency representation into a corresponding discrete-time representation;

means, coupled to the output of said means for transforming said real-valued discrete-frequency representation, for circularly shifting said discrete-time representation;

means, coupled to the output of said means for circularly shifting said discrete-time representation, for applying a shortening window to said discrete-time representation to produce a zero-padded reduced length filter; and

means, coupled to the output of said means for applying a shortening window to said discrete-time representation, for convolving an input signal with said zero-padded reduced length filter.

18. (Previously Presented) The apparatus of claim 17, further including means for circularly shifting said zero-padded reduced length filter to remove leading zeroes.

19. (Previously Presented) The apparatus of claims 17, further including means for transforming said zero-padded reduced length filter into a minimum phase filter.

20. (Previously Presented) The apparatus of claim 17, further including means for performing the convolution in the time domain using the discrete-time representation of said zero-padded reduced length filter.

21. (Previously Presented) The apparatus of claim 17, wherein said means for convolving comprises means for performing a convolution of said input signal in the frequency domain by using an overlap-add method.

22. (Previously Presented) The method of claim 17, wherein said means for convolving comprises means for performing a convolution of said input signal in the frequency domain by using an overlap-save method.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None